LESSON PLAN

NAME OF THE FACULTY: - Suman Chaudhary
DISCIPLINE: - CSE
SEMESTER:- 3rd
SUBJECT-DE
Lesson Plan Duration:- 16 weeks (from September 07 to December 24**)**
Work Load (Lecture/Practical) per week (In hours): Lecture- 03, Practical -03

Week	Theory		Practical	
	Lecture Day	**Topic (Including assignment/test)**	**Practical**	**Topic**
1st	1st	Introduction to Digital electronics	1st	Verification and interpretation of truth tables for AND, OR, NOT NAND, NOR and Exclusive OR (EXOR) and Exclusive NOR(EXNOR) gates
	2nd	Distinction between analog and digital signal.		
	3rd	Applications and advantages of digital signals.		
2nd	1st	Introduction to Binary, octal and hexadecimal number system:	2nd	Realisation of logic functions with the help of NAND or NOR gates
	2nd	conversion from decimal and hexadecimal to binary and vice-versa		
	3rd	Binary addition and subtraction including binary points.		
3rd	1st	1's and 2's complement method of addition/subtraction.	3rd	- To design a half adder using XOR and NAND gates and verification of its operation - Construction of a full adder circuit using XOR and NAND gates and verify its operation
	2nd	Assignment and Revision		
	3rd	Concept of code, weighted and non-weighted codes,		
4th	1st	examples of 8421, BCD, excess-3 and Gray code.	Internal viva for the conducted 3 practical's	
	2nd	Concept of parity, single and double parity and error detection		
	3rd	Assignment and revision		

5th	1st	a) Concept of negative and positive logic	4th	Verification of truth table for positive edge triggered, negative edge triggered, level triggered IC flip-flops (At least one IC each of D latch , D flip-flop, JK flip-flops).
	2nd	Definition, symbols and truth tables of NOT, AND, OR, NAND, NOR gate		
	3rd	Definition, symbols and truth tables of EXOR Gates, NAND and NOR as universal gates		
6th	1st	Introduction to TTL and CMOS logic families	5th	Verification of truth table for encoder and decoder ICs, Mux and DeMux
	2nd	Postulates of Boolean algebra, De Morgan's Theorems.		
	3rd	Implementation of Boolean (logic) equation with gates		
7th	1st	Karnaugh map (upto 4 variables) and simple application in developing combinational logic circuits **Assignment and revision**	6th	To design a 4 bit SISO, SIPO, PISO, PIPO shift registers using JK/D flip flops and verification of their operation.
	2nd	Half adder and Full adder circuit, design and implementation.		
	3rd	4 bit adder circuit, Four bit decoder circuits for 7 segment display and decoder/driver ICs.		
8th	1st	Basic functions and block diagram of MUX and DEMUX with different ICs	Internal viva for the conducted 6 practical's	
	2nd	Basic functions and block diagram of Encoder		
	3rd	Concept and types of latch with their working and applications		
9th	1st	Operation using waveforms and truth tables of RS, flip flops.	7th	To design a 4 bit ring counter and verify its operation
	2nd	Operation using waveforms and truth tables of T, D flip flop		
	3rd			

		Operation using waveforms and truth tables of Master/Slave JK		
10th	1st	Introduction on latch and flip flop	8.	Use of Asynchronous Counter ICs (7490 or 7493)
	2nd	Difference between a latch and a flip flop		
	3rd	Assignment and Revision		
11th	1st	Introduction to Asynchronous and Synchronous counters	Internal viva for the conducted all practical's	
	2nd	Introduction of Binary counters		
	3rd	Divide by N ripple counters,		
12th	1st	Decade counter, Ring counter		
	2nd	Introduction and basic concepts including shift left and shift right.		Revision...
	3rd	Serial in parallel out, serial in serial out, parallel in serial out, parallel in parallel out.		
13th	1st	Universal shift register		
	2nd	Working principle of A/D and D/A converters		
	3rd	Brief idea about different techniques of A/D conversion and study of : Stair step Ramp A/D converter		
14th	1st	Dual Slope A/D converter		
	2nd	Successive Approximation A/D Converter Detail study of : Binary Weighted D/A converter		
	3rd	R/2R ladder D/A converter - Applications of A/D and D/A converter.		
15th	1st	Memory organization, classification of semiconductor memories (RAM, ROM, PROM, EPROM, EEPROM),		
	2nd	static and dynamic RAM, introduction to 74181 ALU IC**L**		
	3rd	Assignment and Revision		
Week 16	1st	**Revision**		

	2nd	**Revision**
	3rd	**Revision**