LESSON PLAN				
Name of Faculty	Miss Neha Midha			
Discipline	Computer Engineering			
Semester	4th Computer Organization 16 WEEKS(March 2021 - July 2021)			
Subject				
Duration				
Work Load	Lecture	3 Lecture per week (1 hour /day)		
Week	Theory			
	Day	Topic		
1st		<u> </u>		
	1st	A brief over view of the subject "Computer organization" and relevance of the studying the subject in Diploma level Program.		
	2nd	CPU Organization : Concept of Registers and General Register Organization		
	3rd	Concept of Stack Organization		
2nd	4th	Concept of Instruction Format and types of instructions, Three, Two, One, Zero Address instruction		
	5th	Addressing modes: Immediate, register, direct, in direct,		
	6th	Addressing modes: relative, indexed.		
3rd	7th	Concept of CPU Design		
	8th	Concept of Micro programmed controlled		
	9th	Concept of Hard wired controlled		
4th	10th	Class Test of CPU Design		
	11th	Concept of Reduced instruction Set Computer		
	12th	Concept of Complex instruction Set Computer		
5th	13th	CISC Characteristics, RICS Characteristics		
	14th	Comparision of RISC & CISC		
	15th	Seminar on Topics , Instruction formats and Addressing modes , CICS, RICS		
6th	16th	Concept of Memory Organization, Memory types		
	17th	Memory Hierarchy		
	18th	ROM and RAM Chips, Concept of Memory Address Map		
7th	19th	Connections of Memory Chips with the CPU		
	20th	Concept and usage of Auxiliary Memories and types		
	21st	Study of Magnetic Disks		
8th	22nd	Study of Magnetic Tapes.		
	23rd	Associative and Cache memory		
	24th	Concept of Virtual Memory		
9th	25th	Concept of Memory Management		
	26th	Memory Management Hardware.		
	27th	Revision of Associative, Cache , Virtual memory		
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10th	28th	Read and Write operation of memory
	29th	Concept of Input/output Organization
	30th	Basic Input out put System BIOS and its Function
11th	31st	Testing and Initialization by BIOS, Configuring the System
	32nd	Concept of Data transfer in Computer System
	33rd	Different modes of Data Transfer : Programmed and DMA
12th	34th	Programmed I/O : Synchronous, asynchronous
	35th	Interrupt initiated I/O
	36th	DMA data transfer
13th	37th	Class Test od I/O Organisation
	38th	Concept of Multi Processor Systems
	39th	Different forms of Parallel Processing
14th	40th	Different forms of Parallel Processingcontinued
	41st	Concept of Parallel processing and Pipe Lines
	42nd	Basic Characteristics of Multiprocessor, General purpose multiprocessors.
15th	43rd	Concept of Interconnection Networks
	44th	, Concept of Time Shared Common Bus
	45th	Concept of Multiport Memory, Cross Bar Switch
16th	46th	Multistage Switching networks and hyper cube structures
	47th	Revision of Previous lectures
	48th	Class Test of unit 4