NAME OF FACULTY: DR. MEENU NAIN

DISCIPLINE: COMPUTER ENGINEERING

SEMESTER: 4TH

SUBJECT: COMPUTER ORGANIZATION

LESSON PLAN DURATION: 16 WEEKS

WORK LOAD (LECTURE/ PRACTICAL): LECTURES-3

| WEEK | | THEORY |
|------------------|---------|---|
| 1st | LECTURE | TOPIC |
| | DAY | |
| | 1 | UNIT 1 HARDWARE ORGANIZATION OF COMPUTER SYSTEM |
| | | CPU organization: general register organization |
| | 2 | stack organization |
| | 3 | instruction formats(three address, |
| 2nd | 1 | two address,one address, |
| | 2 | zero address and RISC instruction) |
| | 3 | Addressing modes: Immediate |
| 3rd | 1 | Register Addressing modes, Direct Addressing modes |
| | 2 | Indirect Addressing modes |
| | 3 | Relative Addressing modes, Indexed Addressing modes |
| 4th | 3 | CPU Design : Micro programmed vs. hard wired control |
| | 1 | Reduced instruction set computers: CISC characteristics |
| | 2 | RISC characteristics, and their comparison |
| 5 th | 1 | UNIT 2 MEMORY ORGANIZATION |
| | | Memory Hierarchy |
| | 2 | RAM chips |
| | 3 | ROM chips |
| 6 th | 1 | Memory address map |
| | 2 | Memory connections to CPU |
| | 3 | Auxillary memory : Magnetic disks |
| 7th | 1 | Magnetic tapes |
| | 2 | Associative memory |
| | 3 | Cache memory |
| 8th | 1 | Virtual memory |
| | 2 | Memory management hardware |
| | 3 | Read and Write operation |
| 9th | 1 | UNIT 3 I/O ORGANIZATION |
| | | Basis Input output system(BIOS) |
| | 2 | Function of BIOS |
| | 3 | Testing |
| 10th | 1 | Initialization |
| | 2 | Configuring the system |
| | 3 | Modes of Data Transfer: |
| | | Programmed I/O |
| 11 th | 1 | Synchronous Data Transfer |
| | 2 | Asynchronous Data Transfer |
| | 3 | Interrupt initiated Data Transfer |
| 12th | 1 | DMA data transfer |

| | 2 | UNIT 4 ARCHITECTURE OF MULTIPROCESSOR SYSTEMS |
|------|---|---|
| | | Forms of parallel processing |
| | 3 | Parallel processing |
| 13th | 1 | Pipelines |
| | 2 | Basic characteristics of multiprocessor |
| | 3 | General purpose multiprocessors |
| 14th | 1 | Interconnection networks : time shared common bus |
| | 2 | Multi port memory |
| | 3 | Cross bar switch |
| 15th | 1 | multi stage switching networks |
| | 2 | Hyper cube structures |
| | 3 | REVISION |
| 16th | 1 | TEST |
| | 2 | REVISION |
| | 3 | REVISION |