LESSON PLAN

NAME OF FACULTY: MRS. SUMAN CHAUDHARY

DISCIPLINE: COMPUTER ENGINEERING

SEMESTER: 3rd

SUBJECT: DIGITAL ELECTRONICS

LESSON PLAN DURATION: 16 WEEKS

WORK LOAD (LECTURE/ PRACTICAL): LECTURES-3, PRACTICALS -3

WEEK	THEORY		PRACTICAL	
1st	**LECTURE DAY**	**TOPIC**	**PRACTICAL DAY/PERIOD**	**TOPIC**
	1	**UNIT 1 Introduction**	1-3	Introduction
	2	Distinction between analog and digital signal		
	3	Applications and advantages of digital signals		
2nd	**1**	**UNIT 2 Number System** Binary, octal and hexadecimal number system: conversion from decimal and hexadecimal to binary vice-versa.	1-3	Introduction
	2	Binary, octal and hexadecimal number system: conversion from decimal and hexadecimal to binary and vice-versa.		
	3	Binary addition and subtraction including binary points. 1's and 2's complement method of addition/subtraction.		
3rd	**1**	**UNIT 3 Codes and Parity** Concept of code, weighted and non-weighted codes	1-3	Introduction
	2	Examples of 8421, BCD, excess-3 and Gray code		
	3	Concept of parity, single and double parity and error detection		
4th	**3**	**UNIT 4 Logic Gates and Families** Concept of negative and positive logic	1-3	Verification and interpretation of truth tables for AND, OR, NOT NAND, NOR and Exclusive OR (EXOR) and Exclusive NOR(EXNOR) gates
	1	Definition, symbols and truth tables of NOT, AND		
	2	OR, NAND, NOR, EXOR Gates		
5th	**1**	NAND and NOR as universal gates	1-3	
	2	Introduction to TTL and CMOS logic families		
	3	**TEST**		
6th	**1**	**UNIT 5 Logic Simplification** Postulates of Boolean algebra, De Morgan's Theorems	1-3	Realization of logic functions with the help of NAND or NOR gate
	2	Implementation of Boolean (logic) equation with gates		
	3	Karnaugh map (upto 4 variables)		
7th	**1**	simple application in developing combinational logic circuits	1-3	
	2	**UNIT 6 Arithmetic circuits**		

		Half adder and Full adder circuit		
	3	design and implementation		
8th	**1**	4 bit adder circuit	1-3	To design a half adder using XOR and NAND gates and verification of its operation
	2	**UNIT 7 Decoders, Multiplexeres, De Multiplexeres and Encoder** Four bit decoder circuits for 7 segment display		
	3	decoder/driver ICs		
9th	**1**	Basic functions and block diagram of MUX	1-3	
	2	DEMUX with different ICs		
	3	Basic functions and block diagram of Encoder		
10th	**1**	**UNIT 8 Latches and flip flops** Concept and types of latch with their working and applications	1-3	Construction of a full adder circuit using XOR and NAND gates and verify its operation
	2	Operation using waveforms and truth tables of RS flip flops		
	3	T, D, Master/Slave JK flip flops		
11th	**1**	Difference between a latch and a flip flop	1-3	
	2	**UNIT 9 Counters** Introduction to Asynchronous and Synchronous counters		
	3	Asynchronous and Synchronous counters		
12th	**1**	Binary counters	1-3	Verification of truth table for positive edge triggered, negative edge triggered, level triggered IC flip-flops (At least one IC each of D latch , D flip-flop, JK flip-flops).
	2	Divide by N ripple counters,		
	3	Decade counter, Ring counter		
13th	**1**	**UNIT 10 Shift Register** Introduction and basic concepts including shift left and shift right.	1-3	Verification of truth table for encoder and decoder ICs, Mux and DeMux
	2	Serial in parallel out, serial in serial out		
	3	Parallel in serial out, parallel in parallel out		
14th	**1**	Universal shift register	1-3	To design a 4 bit SISO, SIPO, PISO, PIPO shift registers using JK/D flip flops and verification of their operation
	2	**UNIT 11 A/D and D/A Converters** Working principle of A/D and D/A converters		
	3	Brief idea about different techniques of A/D conversion and study of : Stair step Ramp A/D converter		
15th	**1**	Dual Slope A/D converter Successive Approximation A/D Converter	1-3	To design a 4 bit ring counter and verify its operation.
	2	Detail study of : Binary Weighted D/A converter, R/2R ladder D/A converter		
	3	Applications of A/D and D/A converter		
16th	**1**	**UNIT 12 Semiconductor Memories** Memory organization, classification of semiconductor memories (RAM, ROM, PROM, EPROM,	1-3	Use of Asynchronous Counter ICs (7490 or 7493)
	2	EEPROM), static and dynamic RAM, introduction to 74181 ALU IC		
	3	**REVISION**		