## Electrical Engineering Department Lesson plan

Name of Faculty	SUCHET KUMARI
Discipline	Electrical Engineering
Semester	Third Sem (3rd sem)
Subject	Analog & Digital Electronics
Lesson Plan Duration	From Sep 2023
Work load [Theory + Practical] Per Week	[03+04]

Week	Day	Theory Topic/ Assignment/ Test	No.	Practical
1 <sup>st</sup>	1	Unit1: Concept of insulators, conductors and semiconductors.	1	To Plot V-I characteristics of a PN junction diode
	2	Intrinsic and extrinsic		
	3	P and N type semiconductor and their conductivity.		
2 <sup>nd</sup>	1	Effect of temperature on conductivity of intrinsic semiconductor	2	To Plot V-I characteristics of a Zener diode
	2	PN junction diode, mechanism of current flow in PN junction,		
	3	forward and reverse biased PN junction, potential barrier,		
3 <sup>rd</sup>	1	drift and diffusion currents, depletion layer	3	Half-wave rectifier circuit using one diode
	2	. V-I characteristics of diodes		
	3	Diode as half-wave, full wave.		
4 <sup>th</sup>	1	Bridge rectifiers	4	Full-wave rectifier circuit using two diodes
	2	Peak Inverse Voltage, rectification efficiencies and ripple factor calculations,		
	3	Concept of filters		
5 <sup>th</sup>	1	Types of diode, characteristics and applications of Zener diodes	5	Observe the output of waveform of Bridge-rectifier circuit using four diodes.
	2	Revision		
	3	Revision		
6 <sup>th</sup>	1	UNIT:2 Concept of a bipolar transistor, PNP and NPN transistors.	6	Plotting of input and output characteristics and calculation of parameters of transistors in CE configuration
	2	CB, CE, CC configurations of a transistor.		
	3	Transistor as an amplifier in CE Configuration,		
7 <sup>th</sup>	1	Current amplification factors,	7	Plotting of input and output characteristics and calculation of parameters of transistors in CB configuration
	2	Comparison of CB, CE and CC Configurations.		

	3	Construction, operation		
8 <sup>th</sup>	1	Characteristics of FETs. FET as an amplifier.	8	Plotting of V-I characteristics of a FET
	2	Construction, operation and characteristics of a MOSFET.		
	3	Comparison of JFET, MOSFET and BJT.		
9 <sup>th</sup>	1	Revision	9	Basic logic operations of AND, OR, NOT gates
	2	Revision		<b>B</b>
	3	UNIT 3 Distinction between analog and digital signal.		
10 <sup>th</sup>	1	Decimal, Binary, octal and hexadecimal number system.	10	Verification of truth tables for NAND, NOR and Exclusive OR (EX-OR) and Exclusive NOR (EX-NOR) gates.
	2	Conversion from decimal and hexadecimal to binary and vice- versa.		
	3	Binary addition		
11 <sup>th</sup>	1	Binary subtraction.	11	Realization of logic functions with the help of NAND or NOR gates
	2	Binary division and multiplication		
	3	Definition, symbols and truth tables of Logic gates		
12 <sup>th</sup>	1	Revision	12	To design a half adder using XOR and NAND gates and verification of its operations
-	2	Revision		
	3	UNIT 4 Difference between Sequential Circuits and combinational ciricuit		
13 <sup>th</sup>	1	Half adder, Full adder	13	Construction of a fu Construction of a full adder circuit using XOR and NAND gates and verify its operation
	2	Mux, De-Mux,		
	3	Encoder and Decoder.		
14 <sup>th</sup>	1	Combinational Circuits like Latch, Flip Flops	14	Verification of truth table for IC flip-flops (At least one IC each of D latch, D flip-flop, JK flip- flops).
	2	Shift registers.		
	3	counters.		
15 <sup>th</sup>	1	A/D Converters	15	Verification of truth table for encoder and decoder ICs
	2	D/A Converters		Verification of truth table for Mux and De-Mux
	3	Applications of A/D and D/A Converters		
	2	<b>Revision of Old Question Papers</b>		
	3	<b>Revision of Old Question Papers</b>		